Session 24 Overview

Multi-GB/s Transceivers

Chair: Robert Payne, *Texas Instruments, Dallas TX*

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Once isolated to optical communication systems, multi-Gb/s serial transceiver technology continues to be deployed in broader applications. The capability to create, consume, and process massive quantities of data in industrial and consumer applications likewise increases the bandwidth requirements for system-to-system, chip-to-chip, and even system-in-a-package (SiP) communications.

An optimized high-speed transceiver technology is required for each of these distinct applications. The tradeoffs between power consumption, data rate, port density, and signal integrity must be examined for each application. For example, in backplane communications, channel count may be limited but robust operation often must be guaranteed in legacy systems which were never intended to carry such high data-rate signals. In contrast, chip-to-chip communications often occur over shorter channels with relatively high signal integrity but a premium is placed on low power consumption.

In backplanes, both linear and decision-feedback varieties of analog equalization have been employed to address the poor signal integrity. Paper 24.1 from TI describes a digital approach to both equalization and clock recovery using a front-end A/D converter operating at 12.5Gs/s and backend digital signal processing. A BER<10^{-15} is achieved in a system with 24dB loss at the Nyquist frequency.

The next three papers describe different approaches to transceivers in 90nm CMOS technology. In Paper 24.2 from Sony and Mixed Signal Systems, 10GHz clocks are driven directly from an LC oscillator to the receiver to avoid the additional power and jitter contributions of clock buffers, resulting under 1ps of recovered clock jitter.

Low power is the focus of Paper 24.3 from Rambus, where a combination of techniques including circuit sharing, resonant clock distribution, and low-swing signaling achieves a power efficiency of 2.2mW/Gb/s in a 6.25Gb/s chip-to-chip transceiver.

The authors of Paper 24.4 from Fujitsu describe an equalizer adaptation technique for a 3.1/10.3Gb/s transceiver that minimizes convergence variations for highly periodic 8B/10B encoded data.

New approaches to >16Gb/s transmitters are presented in Papers 24.5 from National Taiwan U and 24.6 from IBM. The former presents an approach to channel characterization and transmit equalizer configuration using the data channel as part of a voltage-controlled oscillator. The latter presents a voltage-mode approach to a 16Gb/s transmitter that addresses equalization and process tuning and supports DC termination from 0V to V_{DD}.

In Paper 24.7 from UCLA and SST Communications, two techniques for 10Gb/s interconnect are presented for 3D chip integration for SiP applications. The measured performance of both impulse and RF techniques are compared.

24.1 A 12.5Gb/s SerDes in 65nm CMOS Using a Baud-Rate ADC with Digital RX Equalization and Clock Recovery 8:30 AM

M. Harwood, Texas Instruments, Northampton, United Kingdom

A DSP-based low-power 12.5Gb/s SerDes using a baud-rate ADC and a digital data-path is developed for backplane data communication. A digital 2-tap FFE and a 5-tap DFE in the RX provide channel compensation. A BER of $<10^{-15}$ is measured over legacy backplanes with 24dB loss at Nyquist. The power consumption and die area are 330mW and 0.45mm^2 per TX/RX pair.

24.2 A 250mW Full-Rate 10Gb/s Transceiver Core in 90nm CMOS using a Tri-State Binary PD with 100ps Gated Digital Output 9:00 AM

T. Masuda, Sony, Kanagawa, Japan

A full-rate 10Gb/s transceiver core employing a tri-state binary PD with 100ps gated digital output is implemented in a 90nm CMOS process. Direct drive from the VCO is utilized to eliminate the 10GHz clock buffer current. The RX exhibits a recovered-clock jitter of 906fs$_{rms}$ and an input sensitivity of 5.9mV$_{pp}$. The TX generates a jitter of 5mUI$_{rms}$. The chip consumes 250mW.

24.3 A 14mW 6.25Gb/s Transceiver in 90nm CMOS for Serial Chip-to-Chip Communication 9:30 AM

R. Palmer, Rambus, Chapel Hill, NC

A power-efficient 6.25Gb/s transceiver in 90nm CMOS for chip-to-chip communication is presented. It dissipates 2.2mW/Gb/s operating at a BER of $<10^{-15}$ over a channel with -15dB attenuation at 3.125GHz. A shared LC-PLL, resonant clock distribution, a low-swing voltage-mode transmitter, a low-power phase rotator, and a software-based CDR and an adaptive equalizer are used to reduce power.

24.4 A 4-Channel 3.1/10.3Gb/s Transceiver Macro with a Pattern-Tolerant Adaptive Equalizer 10:15 AM

Y. Hidaka, Fujitsu Laboratories of America, Sunnyvale, CA

Fabricated in 90nm CMOS, the chip consumes 545mW and has a pattern-balancing adaptive equalizer that is stable for any data patterns including those with a strong peak component at a single frequency. The adaptive equalizer yields a gain at $f_s/2$ relative to $f_s/16$ varying from -1.7 to 2.2dB for any 8B10B encoded Ethernet frames filled with a fixed data byte.

24.5 A 20Gb/s Broadband Transmitter with Auto-Configuration Technique 10:45 AM

J. Lee, National Taiwan University, Taipei, Taiwan

An adaptive scheme to automatically configure the transmitter at power up without using any additional trace is proposed. Incorporating inverters and proper terminations, the circuit forms a ring oscillator whose frequency is directly related to channel loss. This approach is verified using a 20Gb/s feedforward transmitter and a corresponding receiver.

24.6 A 16Gb/s Source-Series Terminated Transmitter in 65nm CMOS SOI 11:15 AM

C. Menolfi, IBM, Rueschlikon, Switzerland

A half-rate source-series terminated TX, operating at data-rates up to 16Gb/s, targets chip-to-chip on-board interconnects. The TX features a 4-tap FFE, tunable termination, and clock-cleanup circuitry for low duty-cycle distortion, and is capable of driving loads referenced to a variable termination voltage, including Gnd, V_{DD}, and $V_{DD}/2$. Implemented in 65nm SOI, it occupies an area of 230×56μm^2 and draws 57.5mA from a 1V supply at 16Gb/s.

24.7 Two 10Gb/s/pin Low-Power Interconnect Methods for 3D ICs 11:45 AM

Q. Gu, University of California, Los Angeles, CA

Two RF techniques are combined with capacitive coupling interconnect to form ultra-wide-bandwidth impulse interconnect and RF interconnect in 3D IC technology. They achieve 10Gb/s/pin and 11Gb/s/pin transmission with 2.7mW/pin and 4.35mW/pin power consumption, respectively, using the MIT Lincoln Lab 3D 0.18μm CMOS, an 8× improvement over previous work.